Spin Wave Approximate Computing

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Outline

- ❑Introduction
- ❑Spin Wave Approximate Full Adder
- ❑Simulation Results and Performance Evaluation
- ❑Spin Wave Approximate Multiplier
- ❑Simulation Results and Performance Evaluation
- ❑Conclusions

Introduction

- CMOS downscaling became more and more difficult due to various technological hurdles.

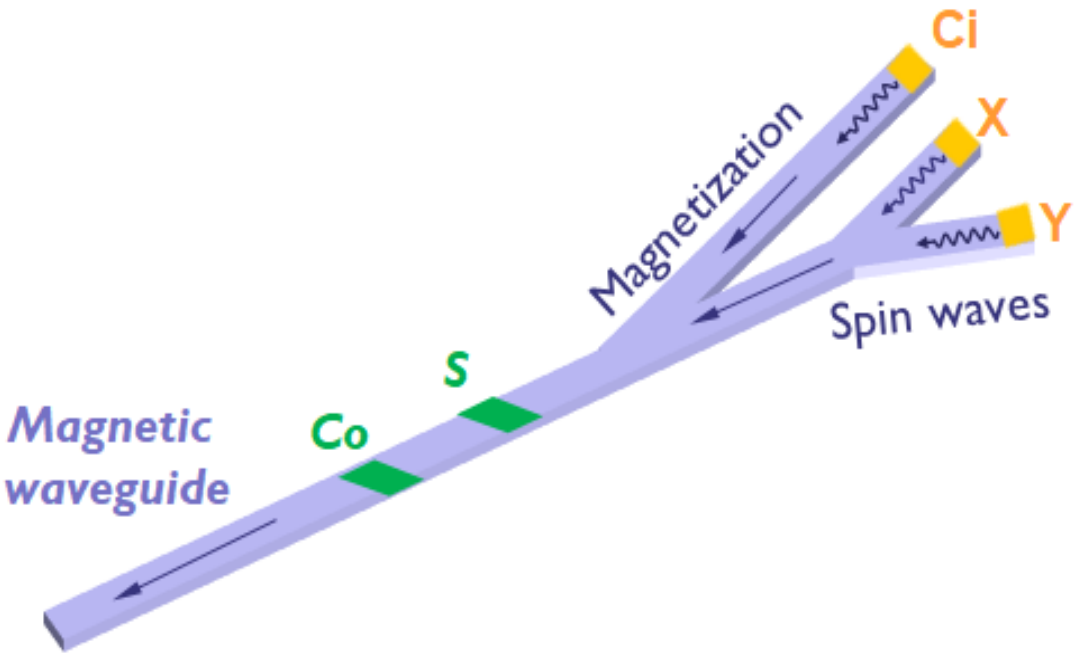
- Spin Wave (SW) based technology stands apart as a promising alternative avenue because:
  - Wavelength: down to nm.
  - Frequency: up to THz.
  - Energy: $E_m << k_B T$.
  - Acceptable delay.
  - Intrinsic data parallelism.

Accurate vs Approximate SW Computing

- Accurate computing give us accurate results while consuming large power, delay and area, but many applications is error tolerant such as:
  - Multimedia processing.
  - Machine learning.
  - Signal processing.
  - Scientific computing, etc. Google is using this approach in their Tensor processing units (TPU, a custom ASIC).
- Therefore, approximate computing can be used instead of the accurate computing which will result in saving power, delay and area.

SW Approximate Full Adder

- Co=S'=MAJ(X,Y,Ci)
- SWs have constructive interference if SWs in-phase.
- SWs have destructive interference if SWs out-of-phase.
- Co is the non-inverted output.
- S is the inverted output.



Truth Table

X	Y	Ci	Sac	Sap	Co
0	0	0	0	**1**	0
0	0	1	1	1	0
0	1	0	1	1	0
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	1	0	0	0	1
1	1	1	1	**0**	1

Parameters

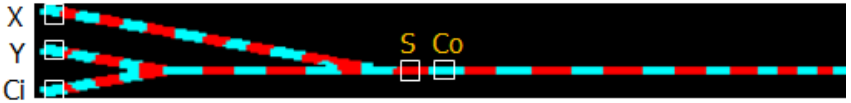
- Saturation magnetization: 1.1 MA/m.
- Damping constant: 0.004.
- Exchange constant: 18.5 pJ/m3.
- Thickness: 1 nm.
- Width =50nm.
- Frequency=10GHz.
- No external field is applied as the shape anisotropy is strong enough to push the magnetization in the plane along the waveguide length. This configuration allows the propagation of backward volume spin waves.

T. Devolder, J.-V. Kim, F. Garcia-Sanchez, J. Swerts, W. Kim, S. Couet, G. Kar, and A. Furnemont, “Time-resolved spin-torque switching in mgo-based perpendicularly magnetized tunnel junctions,” Phys. Rev. B, vol. 93, p. 024420, Jan 2016. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.93.024420

Proposed Approximate FA Simulation Results

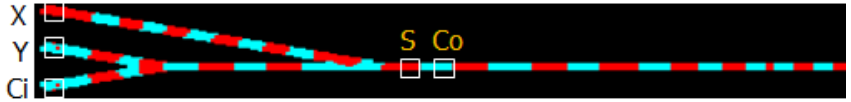
- Red presents logic 1, which presents a phase of π, blue presents logic 0 which presents phase 0.

{X,Y,Cin}={0,0,0}->Co=0



a)

{X,Y,Cin}={0,0,1}->Co=0

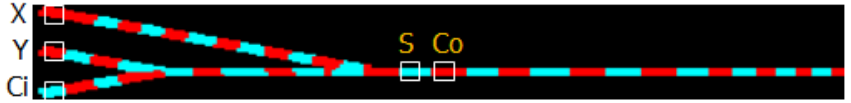


b)

{X,Y,Cin}={0,1,0}->Co=0

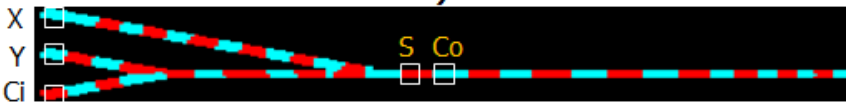
c)

{X,Y,Cin}={0,1,1}->Co=1



d)

{X,Y,Cin}={1,0,0}->Co=0



e)

{X,Y,Cin}={1,0,1}->Co=1

f)

{X,Y,Cin}={1,1,0}->Co=1

g)

{X,Y,Cin}={1,1,1}->Co=1

h)

Performance Evaluation

Technology	Type	Error Rate (%)	Energy (fJ)	Delay (ns)	Device No.
CMOS [1]	Accurate	0	0.066	0.005	28
CMOS [2]	Accurate	0	0.14	0.12	24
	Approximate	25	0.077	0.1	14
MTJ-based [3]	Accurate	0	5685	3.02	29
MTJ-based [4]	Approximate	50	5109	3.02	25
	Approximate	50	2471	3.15	29
SHE-based [5]	Accurate	0	4970	7	26
DWM [6]	Accurate	0	74.5	0.877	26
Spin-CMOS [7]	Accurate	0	166.7	3	34
	Approximate	25	58	2	34
Spin Wave	Accurate	0	0.1	2.86	7
	Approximate	25	0.062	1.84	5

- AFA saves 35% and 6% energy when compared with the state-of-the-art SW and 7nm CMOS, respectively, and 56% and 20% in comparison with accurate and approximate 45nm CMOS, respectively, and saves more than 2 orders of magnitude when compared with accurate SHE, and accurate and approximate DWM, MTJ, and Spin-CMOS FAs. Moreover, it achieves the same error rate as approximate 45nm CMOS and Spin-CMOS FA whereas it exhibits 50% less error rate than approximate DWM FA, and requires at least 29% less chip real-estate in comparison with the other state-of-the-art designs.

[1] T. F. Canan, S. Kaya, A. Karanth and A. Louri, "Ultracompact and Low-Power Logic Circuits via Workfunction Engineering," in *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 5, no. 2, pp. 94-102, Dec. 2019,.
[2] V. Gupta, D. Mohapatra, A. Raghunathan, and K. Roy, “Low-power digital signal processing using approximate adders,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 32, no. 1, pp. 124–137, 2013.
[3] S. Matsunaga, J. Hayakawa, S. Ikeda, K. Miura, H. Hasegawa, T. Endoh, H. Ohno, and T. Hanyu, “Fabrication of a nonvolatile full adder based on logic-in-memory architecture using magnetic tunnel junctions,” Applied Physics Express, vol. 1, no. 9, p. 091301, 2008.
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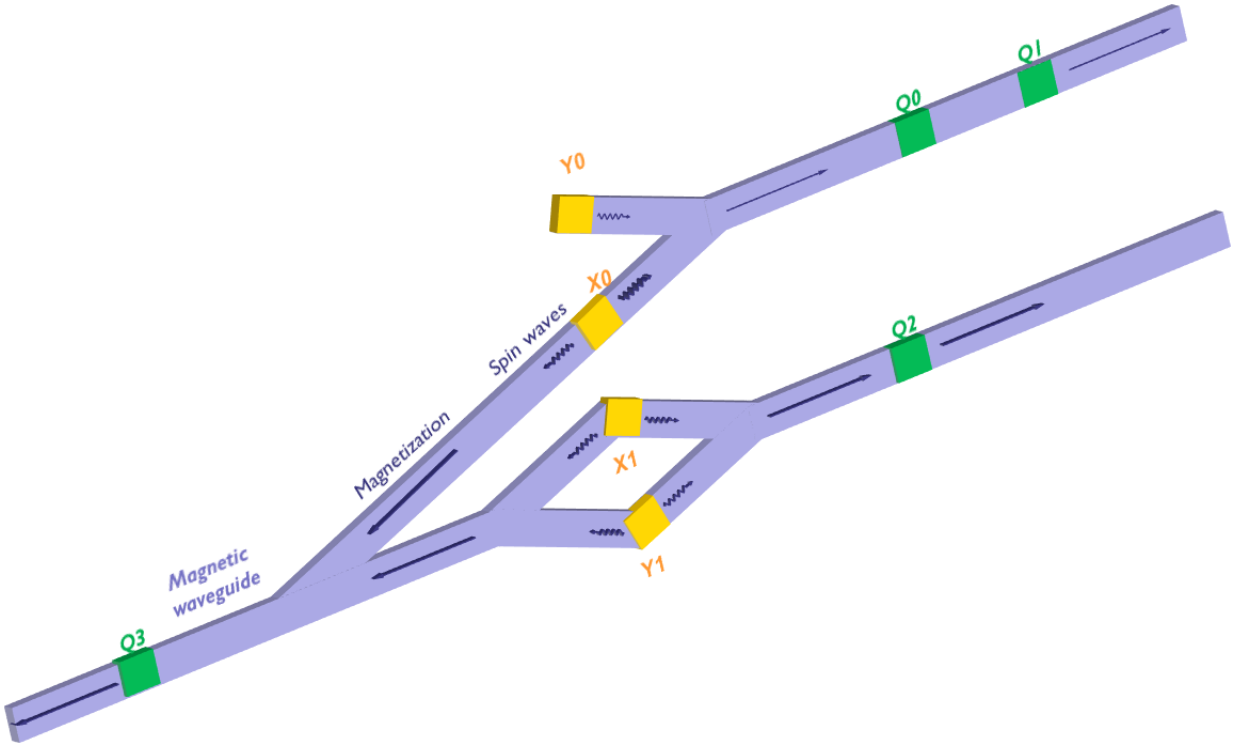
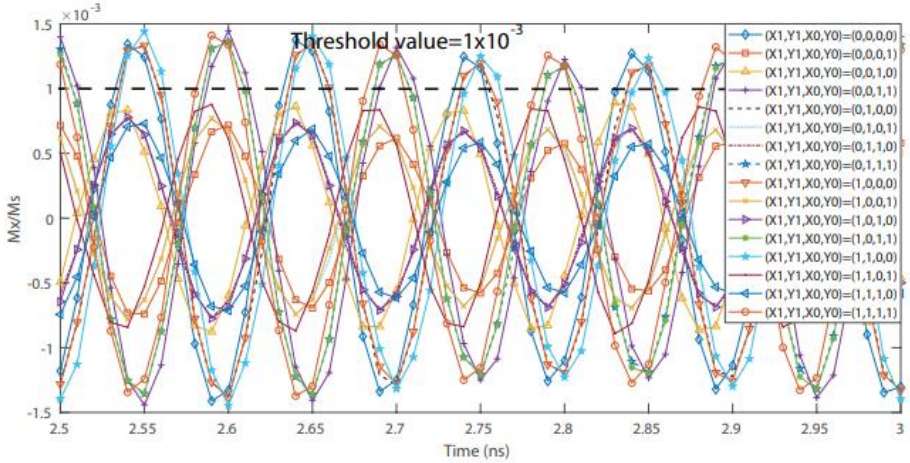
SW Approximate multiplier

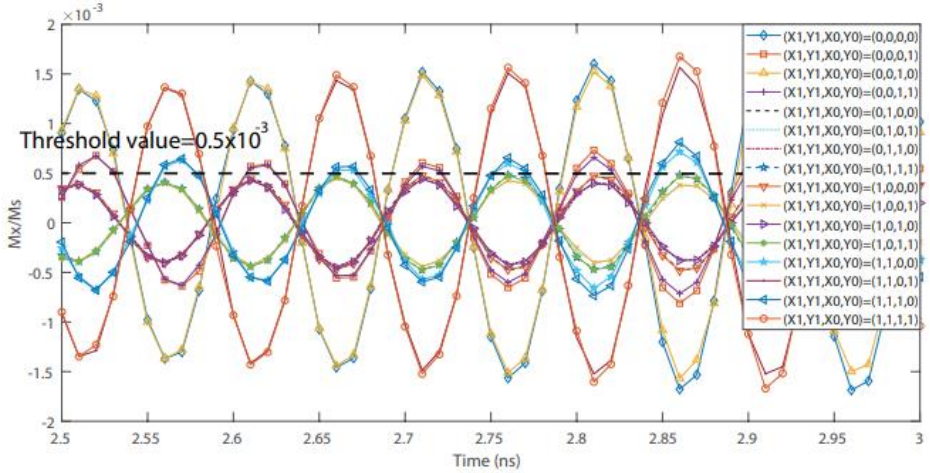
- Q0=Q1=AND(X0,Y0).
- Q2=AND(X1,Y1).
- Q3=AND(X0,X1,Y1).
- SWs have constructive interference if SWs in-phase.
- SWs have destructive interference if SWs out-of-phase.
- Outputs are detected based on threshold.



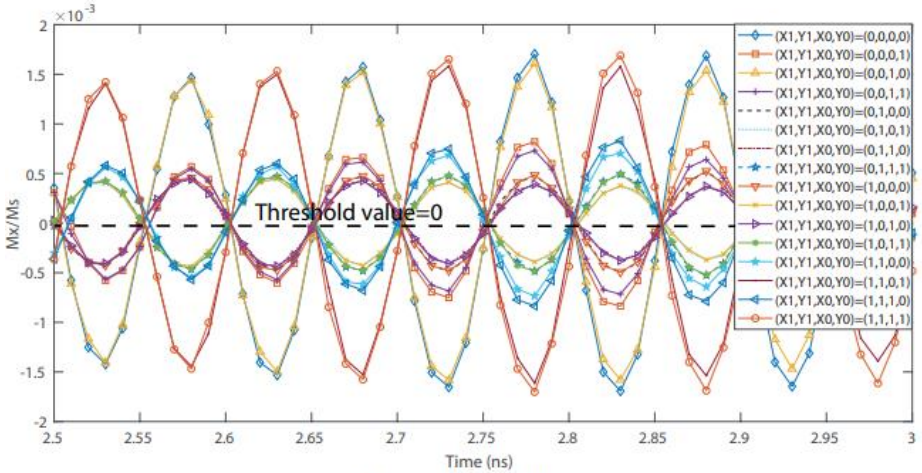
SW Approximate Multiplier Outputs Magnetization



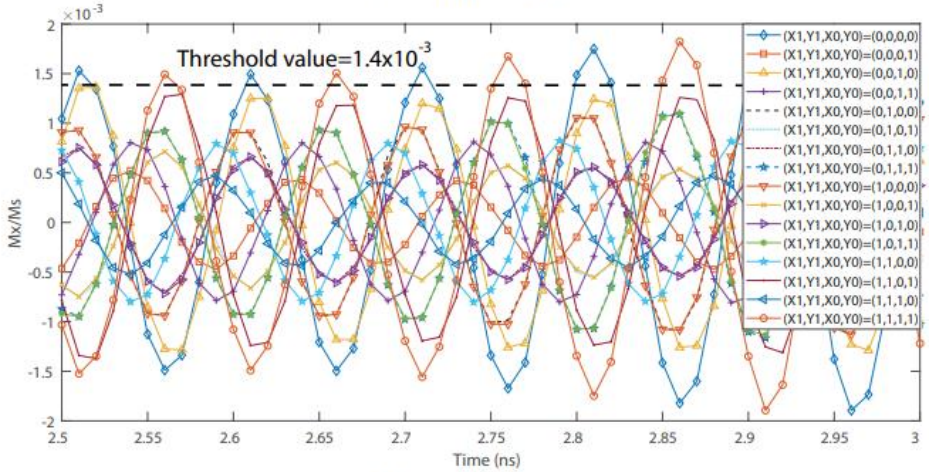
Normalized Q_0.



Normalized Q_2.



Normalized Q_1.



Normalized Q_3.

Performance Evaluation

Designs	Type	Average Error Rate (%)	Energy (aJ)	Delay (ns)	Device No.
CMOS	Accurate [1]	0	959	0.1	52
	Approximate [2]	38	300	0.06	30
Spin Wave	Accurate	0	320	21	22
	Approximate	25	115	3.6	8

- AMUL energy consumption is at least 2.5x smaller the one of state-of-the-art accurate SW designs and 16nm CMOS accurate and approximate designs. Moreover, AMUL exhibits an error rate of 25%, while the approximate CMOS MUL one of 38%.

[1] T. F. Canan, S. Kaya, A. Karanth and A. Louri, "Ultracompact and Low-Power Logic Circuits via Workfunction Engineering," in *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 5, no. 2, pp. 94-102, Dec. 2019, doi: 10.1109/JXCDC.2019.2962494.
[2] V. Gupta, D. Mohapatra, A. Raghunathan, and K. Roy, “Low-power digital signal processing using approximate adders,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 32, no. 1, pp. 124–137, 2013.

Conclusions

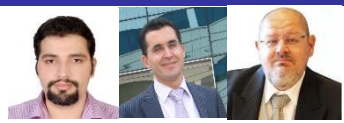
- We developed SW approximate energy efficient spin-wave based Full Adder (AFA) and a 2-bit inputs multiplier (AMUL).
- Both designs were validated by means of MuMax simulations.

- AFA saves 35% and 6% energy when compared with the state-of-the-art SW and 7nm CMOS, respectively, and 56% and 20% in comparison with accurate and approximate 45nm CMOS, respectively, and saves more than 2 orders of magnitude when compared with accurate SHE, and accurate and approximate DWM, MTJ, and Spin-CMOS FAs. Moreover, it achieves the same error rate as approximate 45nm CMOS and Spin-CMOS FA whereas it exhibits 50% less error rate than approximate DWM FA, and requires at least 29% less chip real-estate in comparison with the other state-of-the-art designs.

- At its turn, AMUL energy consumption is at least 2.5x smaller the one of state-of-the-art accurate SW designs and 16nm CMOS accurate and approximate designs. Moreover, AMUL exhibits an error rate of 25%, while the approximate CMOS MUL one of 38%.

CHIRON Team

- TU Delft: Abdulqader Mahmoud, Said Hamdioui, Sorin Cotofana



- IMEC: Frederic Vanderveken, Florin Ciubotaru, Christoph Adelmann

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- CHIRON Webpage:
- https://www.chiron-h2020.eu/

Relevant publications

- A. Mahmoud, N. Cucu-Laurenciu, F. Vanderveken, F. Ciubotaru, C. Adelmann, S. Cotofana, and S. Hamdioui, "Would Magnonic Circuits Outperform CMOS Counterparts?" In Proceedings of the Great Lakes Symposium on VLSI 2022 (GLSVLSI '22), June 6–8, 2022, Irvine, CA, USA. ACM, New York, NY, USA, 5 pagesA. V. Chumak et al., "Roadmap on Spin-Wave Computing," in IEEE Transactions on Magnetics, doi: 10.1109/TMAG.2022.3149664.
- A. Mahmoud, F. Vanderveken, F. Ciubotaru, C. Adelmann, S. Hamdioui and S. Cotofana, "Spin Wave Based Approximate Computing," in IEEE Transactions on Emerging Topics in Computing, doi: 10.1109/TETC.2021.3136299.
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- A. Barman, G. Gubbiotti, [...], C. Adelmann, S. Cotofana, et al., The 2021 magnonics roadmap, Journal of Physics: Condensed Matter. 2021 Aug 18;33(41):413001.
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- A. N. Mahmoud, F. Vanderveken, C. Adelmann, F. Ciubotaru, S. Hamdioui and S. Cotofana, "Multifrequency Data Parallel Spin Wave Logic Gates," in IEEE Transactions on Magnetics, vol. 57, no. 5, pp. 1-12, May 2021, Art no. 3401012, doi: 10.1109/TMAG.2021.3062022.
- A. Mahmoud, F. Ciubotaru, F. Vanderveken, A. V. Chumak, S. Hamdioui, C. Adelmann, and S. Cotofana , "Introduction to spin wave computing", Journal of Applied Physics 128, 161101 (2020) https://doi.org/10.1063/5.0019328
- A. Mahmoud, F. Vanderveken, C. Adelmann, F. Ciubotaru, S. Hamdioui and S. Cotofana, "4-output Programmable Spin Wave Logic Gate," 2020 IEEE 38th International Conference on Computer Design (ICCD), 2020, pp. 332-335, doi: 10.1109/ICCD50377.2020.00062.
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Thank you

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